This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A mixer circuit for reducing the power level of spurious output signals, the mixer comprising:

a first mixer stage which includes a mixer with first and second input ports and an a first output port;

a second mixer stage which includes a second mixer with third and fourth ~~forth~~ input ports and a second output port, said first input port electrically coupled to one or the other of said third and fourth input ports;

a phase modulator for phase modulating a first local oscillator signal, modulated by a pseudorandom code, said phase modulator electrically coupled to one or the other of said first and second input ports; and

an inverse phase modulator for inverse phase modulating a second local oscillator signal, modulated by said pseudorandom code, said inverse phase modulator electrically coupled to the other of said third and fourth input ports.

2. (Original) The mixer circuit as recited in claim 1, wherein said phase modulator is a phase shift keying (PSK) modulator.

3. (Original) The mixer circuit as recited in claim 2, wherein said inverse phase modulator is a phase shift keying (PSK) modulator.

4. (Currently Amended) The mixer circuit as recited in claim 2, wherein said phase modulator is a first direct sequence binary phase shift keying (BPSK) modulator modulated according to a pseudorandom ~~psuedorandom~~ number (PN) code and said mixer circuit includes a PN code generator for generating said PN code.

5. (Original) The mixer circuit as recited in claim 4, wherein said inverse phase modulator is a second direct sequence binary phase shift keying modulator modulated according to said PN code.

6. (Original) The mixer circuit as recited in claim 1, further including an intermediate filter coupled between said first output port and one of said third and fourth input ports.

7-11 (Cancelled)

12. (Original) The mixer as recited in claim 1, wherein said modulator and said inverse modulator are configured for QPSK modulation.

13. (Original) The mixer as recited in claim 1, wherein said modulator and said inverse modulator are configured for PSK modulation.

14. (Original) The mixer as recited in claim 1, wherein said modulator and said inverse modulator are configured for M-ary modulation techniques.

15. The mixer as recited in claim 1, wherein said modulator and said inverse modulator are configured for GMSK modulation techniques.

16-27. (Canceled).

28. (Currently Amended) A method of reducing the power levels of spurious output signals at the output of a mixer circuit comprising the steps of:

(a) providing a two stage mixer including first and second mixer each having a local oscillator port, an input port for receiving first and second local oscillator signals;

(b) phase modulating the first local oscillator signal with a pseudorandom code,; and

(c) inverse phase modulating the second local oscillator signal with said pseudorandom code,.

29. (Original) The method as recited in claim 28, wherein modulating and inverse modulating in steps (b) and (c) are accomplished by BPSK modulation techniques.

30. (Original) The method as recited in claim 28, wherein modulating and inverse modulating in steps (b) and (c) are accomplished by QPSK modulation techniques.

31. (Original) The method as recited in claim 28, wherein modulating and inverse modulating in steps (b) and (c) are accomplished by GMSK modulation techniques.

32. (Original) The method as recited in claim 28, wherein modulating and inverse modulating in steps (b) and (c) are accomplished by M-ary modulation techniques.